and a p-channel TFT, characterized in that:

the CMOS circuit has a structure that an active layer is sandwiched by a first wiring line and a second wiring line through an insulating layer in only the n-channel TFT; and

the second wiring line has a portion of a laminated

structure of a first conductive layer and a second conductive layer, and a portion of a structure in which a third conductive layer is wrapped by the first conductive layer and the second conductive layer.

31. A semiconductor device according to claim 30, characterized in that the third conductive layer has a lower resistance value than a first conductive layer or the second conductive layer.

32. A semiconductor device according to claim 30, characterized in that the first wiring line or the second wiring line is a conductive film mainly containing an element selected from the group consisting of tantalum (Ta), titanium (Ti), tungsten (W), molybdenum (Mo), and silicon (Si), or an alloy film or silicide film containing the above elements in combination.

33. A semiconductor device according to claim 30, characterized in that the third wiring line is a conductive film mainly containing aluminum (Al) or copper (Cu).

34. A semiconductor device including a pixel matrix circuit that has a pixel TFT formed by an n-channel TFT and a storage capacitor, characterized in that:

the pixel TFT has a structure that an active layer is sandwiched by a first wiring line and a second wiring line

through an insulating layer,

the active layer includes a low concentration impurity region that is in contact with the channel formation region; and

the low concentration impurity region is formed to overlap the first wiring line and not to overlap the second wiring line.

35. A semiconductor device according to claim 34, characterized in that the first wiring line is kept at the ground electric potential or at the source power supply electric potential.

36. A semiconductor device according to claim 34, characterized in that the first wiring line is kept at the floating electric potential.

37. A semiconductor device including a pixel matrix circuit that has a pixel TFT formed by an n-channel TFT and a storage capacitor, characterized in that:

the pixel TFT has a structure that an active layer is sandwiched by a first wiring line and a second wiring line through an insulating layer,

the second wiring line has a portion of a laminated structure of a first conductive layer and a second conductive layer, and a portion of a structure in which a third conductive layer is wrapped by the first conductive layer and the second conductive layer.

38. A semiconductor device according to claim 37, characterized in that the third conductive layer has a lower resistance value than the first conductive layer or the second conductive layer.

39. A semiconductor device according to claim 37, characterized in that the first wiring line or the second wiring line is a conductive film mainly containing an element selected from the group consisting of tantalum (Ta), titanium (Ti), tungsten (W), molybdenum (Mo), and silicon (Si), or an alloy film or silicide film containing the above elements in combination.

40. A semiconductor device according to claim 37, characterized in that the third wiring line is a conductive film mainly containing aluminum (Al) or copper (Cu).

41. A semiconductor device having a pixel matrix circuit and a driver circuit that are formed on the same substrate, characterized in that:

a pixel TFT included in the pixel matrix circuit and an n-channel TFT included in the driver circuit have a structure that an active layer is sandwiched by a first wiring line and a second wiring line through an insulating layer; and

the first wiring line connected to the pixel TFT is kept at the fixed electric potential or the floating electric potential, and the first wiring connected to the n-channel TFT included in the driver circuit is kept at the same level of electric potential as the second wiring line connected to the n-channel TFT included in the said driver circuit.

42. A semiconductor device according to claim 41, characterized in that the active layer includes a low concentration impurity region that is in contact with the channel formation region; and

the low concentration impurity region is formed to overlap the first wiring line and not to overlap the second wiring line.

43. A semiconductor device according to claim 41, characterized in that the second wiring line has a portion of a laminated structure of a first conductive layer and a second conductive layer, and a portion of a structure in which a third conductive layer is wrapped by the

first conductive layer and the second conductive layer.

44. A semiconductor device according to claim 41, characterized in that the third conductive layer has a lower resistance value than a first conductive layer or the second conductive layer.

45. A semiconductor device according to claim 41, characterized in that the first wiring line or the second wiring line is a conductive film mainly containing an element selected from the group consisting of tantalum (Ta), titanium (Ti), tungsten (W), molybdenum (Mo), and silicon (Si), or an alloy film or silicide film containing the above elements in combination.

46. A semiconductor device according to claim 41, characterized in that the third wiring line is a conductive film mainly containing aluminum (Al) or copper (Cu).

47. A semiconductor device, characterized in that the semiconductor device according to any one of claims 28 to 46 is an active matrix liquid crystal display or an active matrix EL display.

48. A semiconductor device, characterized in that the semiconductor device according to any one of claims 28 to 46 is a video camera, a digital camera, a projector, a projection TV, a goggle type display, an automobile navigation system, a personal computer, or a portable information terminal.

49. A manufacturing method of a semiconductor device including a CMOS circuit formed by an n-channel TFT and a p-channel TFT comprising:

a process of forming a first wiring line on a substrate,

a process of forming a first insulating layer on the first wiring line,

a process of forming active layers, an active layer of the n-channel TFT and an active layer of the p-channel TFT, on the first insulating layer,

a process of forming a second insulating layer to overlap the active layer of the n-channel TFT and the active layer of the p-channel layer, and

a process of forming a second wiring line on the second insulating layer; and

characterized in that the first wiring line is formed to cross only the active layer of the n-channel TFT.

50. A manufacturing method of a semiconductor device according to claim 49, characterized in that the second wiring line has a portion of a laminated structure of a first conductive layer and a second conductive layer, and a portion of a structure in which a third

conductive layer is wrapped by the first conductive layer and the second conductive layer.

51. A manufacturing method of a semiconductor device including a CMOS circuit formed by an n-channel TFT and a p-channel TFT comprising:

a process of forming a first wiring line on a substrate,

a process of forming a first insulating layer on the first wiring line,

a process of forming active layers, an active layer of the n-channel TFT and an active layer of the p-channel TET,

on the first insulating layer,

a process of forming a second insulating layer to overlap the active layer of the n-channel TFT and the active layer of the p-channel layer,

a process of forming a first conductive layer on the second insulating layer,

a process of forming a patterned third conductive layer on the first conductive layer, and

a process of forming a second conductive layer to overlap the third conductive layer; and

characterized in that the first wiring line is formed to cross only the active layer of the n-channel TFT.

52. A manufacturing method of a semiconductor device according to claim 50 or 51, characterized in that a material with a lower resistance value than the first conductive layer or the second conductive layer is used as the third conductive layer.

53. A manufacturing method of a semiconductor device according to claim 50 or 51, characterized in that the first wiring line or the second wiring line is a conductive film mainly containing an element selected from the group consisting of tantalum (Ta), titanium (Ti), tungsten (W), molybdenum (Mo), and silicon (Si), or an alloy film or silicide film containing the above elements in combination.

54. A manufacturing method of a semiconductor device according to claim 50 or 51, characterized in that the third conductive layer is a conductive film mainly containing aluminum (Al) or copper (Cu).